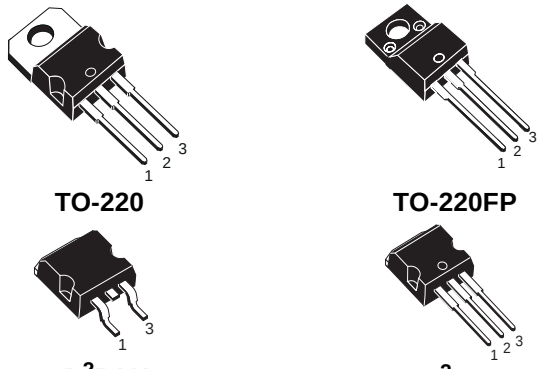
STP11NM60 - STP11NM60FP
STB11NM60 - STB11NM60-1

N-CHANNEL 600V - 0.4Ω-11A TO-220/TO-220FP/D²PAK/I²PAK
MDmesh™ Power MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP11NM60	600 V	< 0.45 Ω	11 A
STP11NM60FP	600 V	< 0.45 Ω	11 A
STB11NM60	600 V	< 0.45 Ω	11 A
STB11NM60-1	600 V	< 0.45 Ω	11 A

- TYPICAL R_{DS}(on) = 0.4Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE



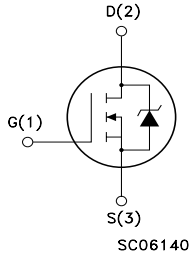
DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP(B)11NM60(-1)	STP11NM60FP	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	600		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	600		V
V_{GS}	Gate- source Voltage	±30		V
I_D	Drain Current (continuous) at T_C = 25°C	11	11 (*)	A
I_D	Drain Current (continuous) at T_C = 100°C	7	7 (*)	A
I_{DM} (•)	Drain Current (pulsed)	44	44 (*)	A
P_{TOT}	Total Dissipation at T_C = 25°C	160	35	W
	Derating Factor	1.28	0.28	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	15		V/ns
V_{ISO}	Insulation Winthstand Voltage (DC)	--	2500	V
T_{stg}	Storage Temperature	–65 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

(•)Pulse width limited by safe operating area

(*)Limited only by maximum temperature allowed

(1)I_{SD}<11A, di/dt<400A/µs, V_{DD}<$V_{(BR)DSS}$, T_J<T_{JMAX}

THERMAL DATA

			TO-220/D²PAK/I²PAK	TO-220FP	
Rthj-case	Thermal Resistance Junction-case	Max	0.78	3.57	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	5.5	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	350	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 5.5A		0.4	0.45	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 5.5A		5.2		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		1000		pF
C_{oss}	Output Capacitance			230		pF
C_{rss}	Reverse Transfer Capacitance			25		pF
$C_{oss\ eq.}$ (2)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 480V		100		pF
R_G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.6		Ω

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 300V, I_D = 5.5A		20		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		20		ns
Q_g	Total Gate Charge	V_{DD} = 400V, I_D = 11A,		30		nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10V		10		nC
Q_{gd}	Gate-Drain Charge			15		nC

SWITCHING OFF

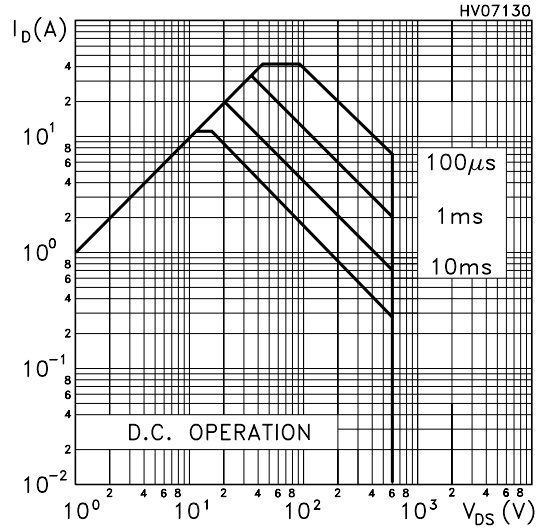
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 400V, I_D = 11A,		6		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		11		ns
t_c	Cross-over Time			19		ns

SOURCE DRAIN DIODE

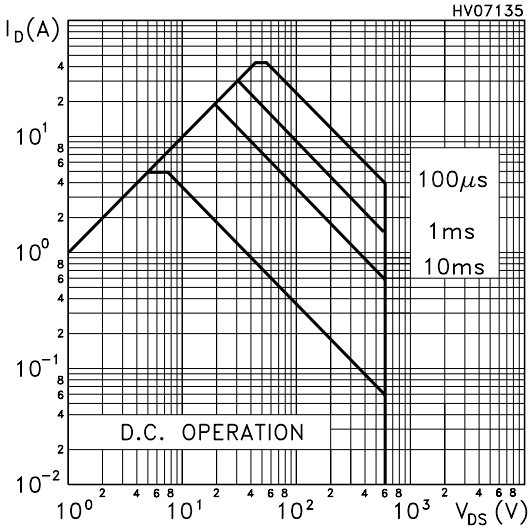
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				11	A
I_{SDM} (2)	Source-drain Current (pulsed)				44	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 11A, V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 11A, di/dt = 100A/µs,		390		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 100 V, T_j = 25°C		3.8		µC
I_{rrm}	Reverse Recovery Current	(see test circuit, Figure 5)		19.5		A
t_{rr}	Reverse Recovery Time	I_{SD} = 11A, di/dt = 100A/µs,		570		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 100 V, T_j = 150°C		5.7		µC
I_{rrm}	Reverse Recovery Current	(see test circuit, Figure 5)		20		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

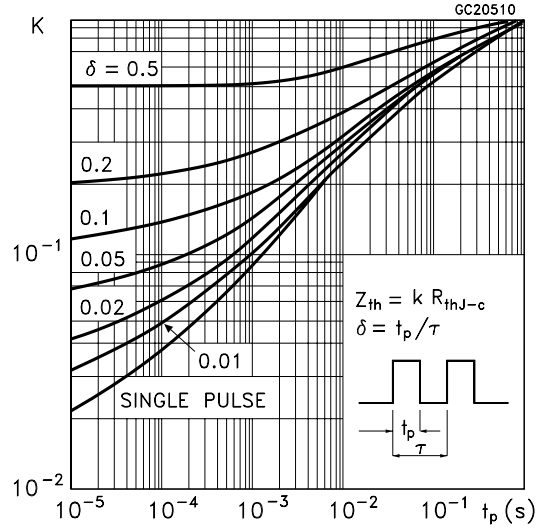
Safe Operating Area for TO-220/D2PAK/I2PAK



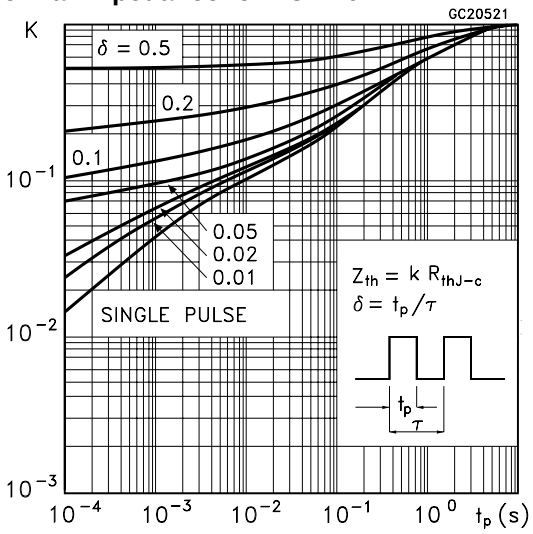
Safe Operating Area for TO-220FP



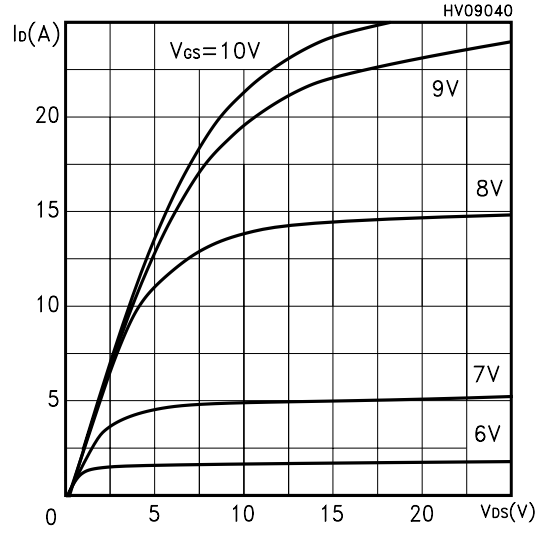
Thermal Impedance for TO-220/D2PAK/I2PAK



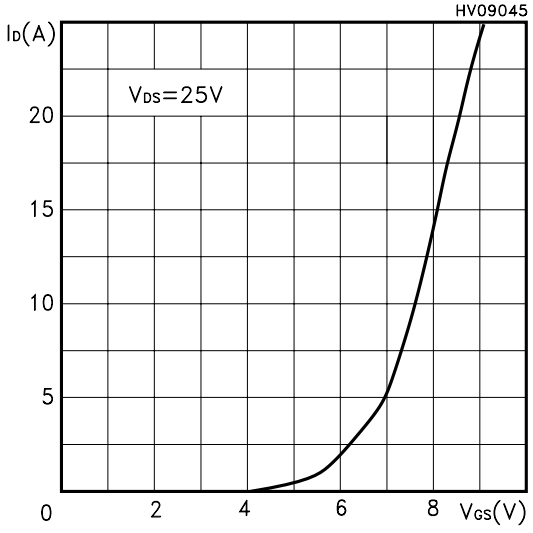
Thermal Impedance for TO-220FP



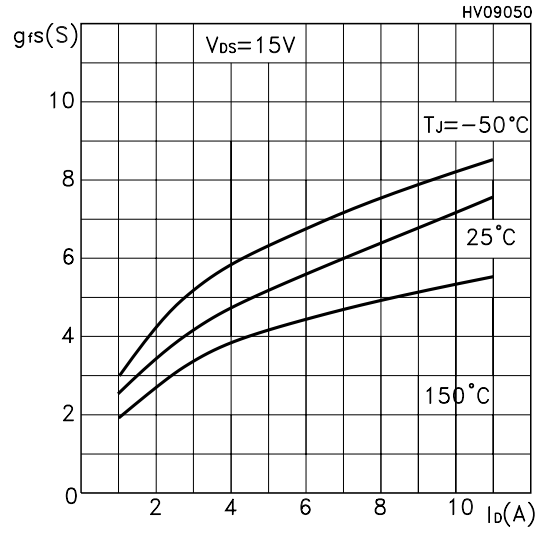
Output Characteristics



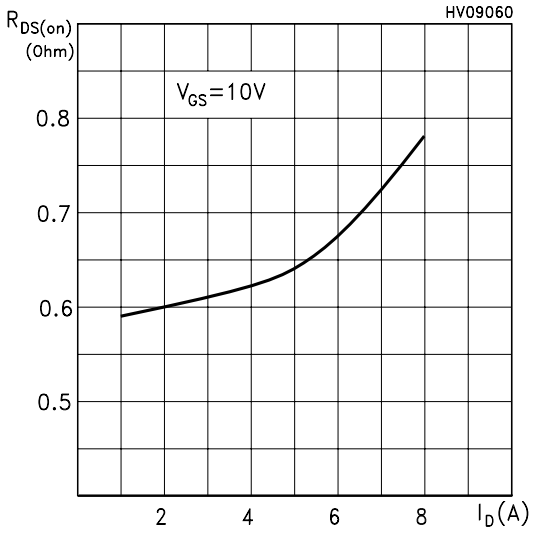
Transfer Characteristics



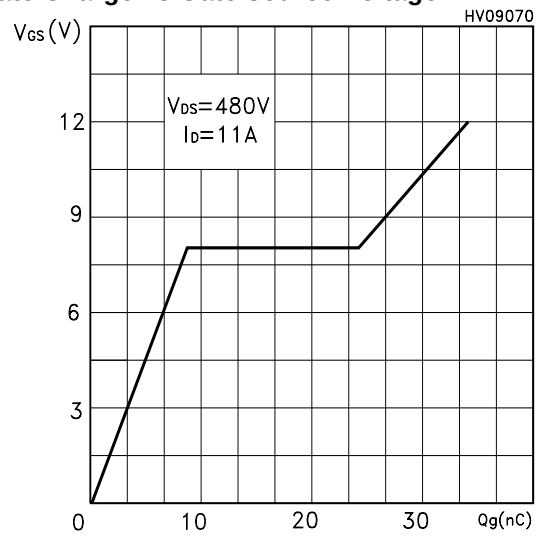
Transconductance



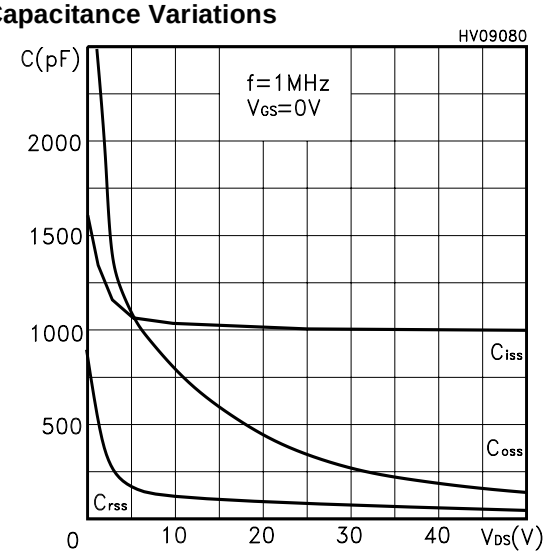
Static Drain-source On Resistance



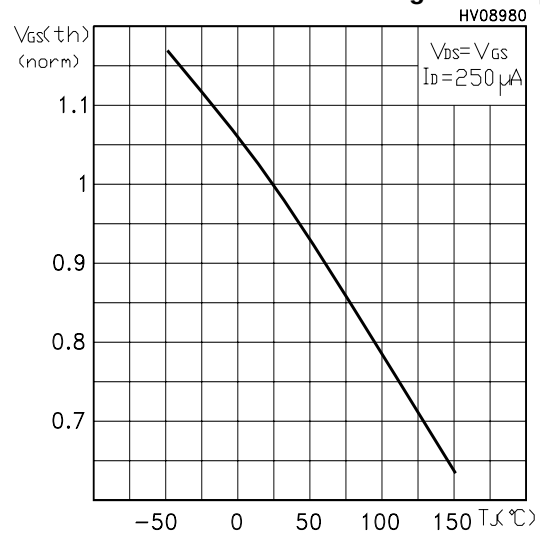
Gate Charge vs Gate-source Voltage



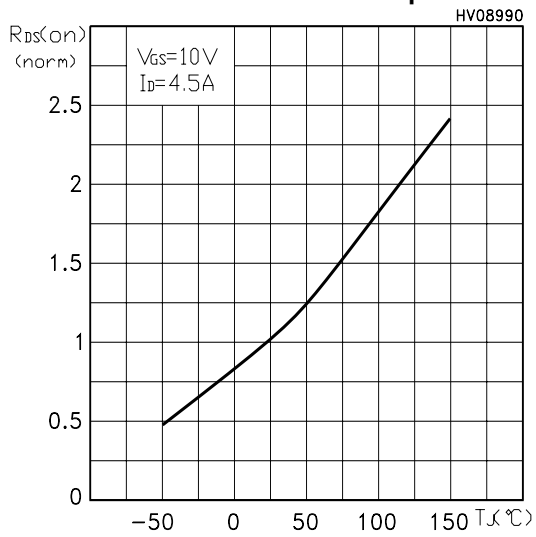
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

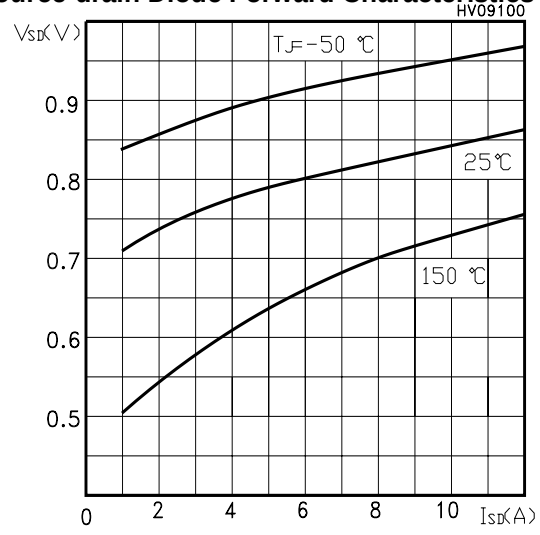


Fig. 1: Unclamped Inductive Load Test Circuit

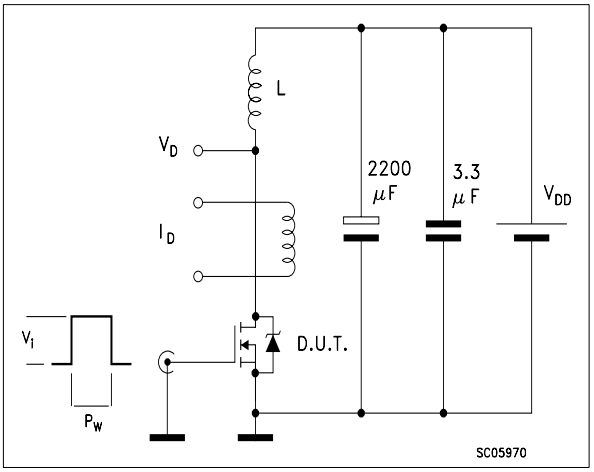


Fig. 2: Unclamped Inductive Waveform

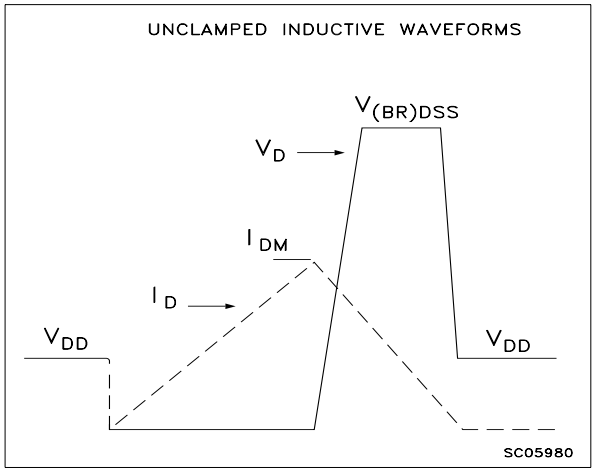


Fig. 3: Switching Times Test Circuit For Resistive Load

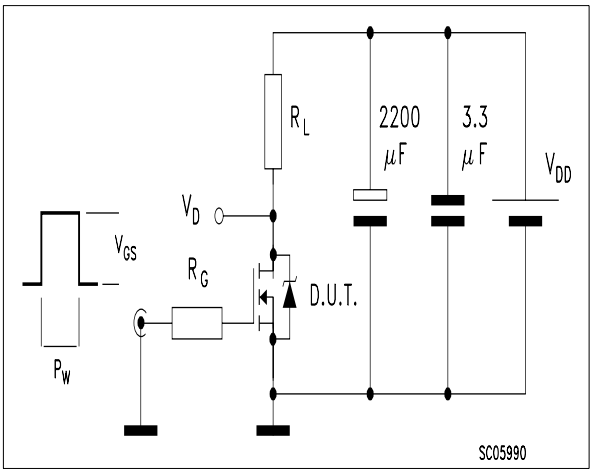


Fig. 4: Gate Charge test Circuit

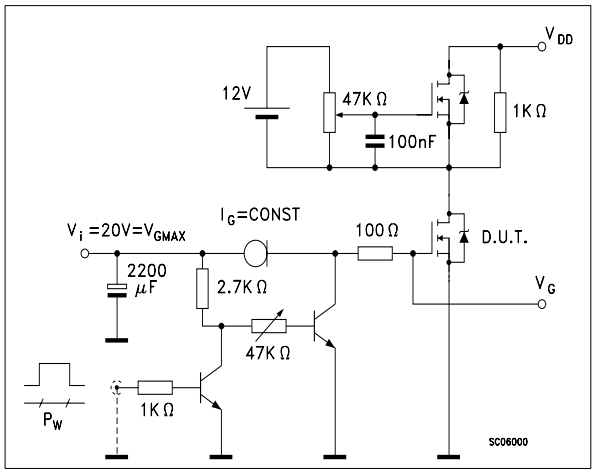


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times