INTEGRATED CIRCUITS

DATA SHEET

TDA6107JF
Triple video output amplifier

Product specification 2002 Oct 18

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Triple video output amplifier TDA6107JF

FEATURES

- Typical bandwidth of 5.5 MHz for an output signal of 60 V (p-p)
- High slew rate of 900 V/µs
- No external components required
- Very simple application
- Single supply voltage of 200 V
- Internal reference voltage of 2.5 V
- Fixed gain of 50
- Black-Current Stabilization (BCS) circuit with voltage window from 1.8 to 6 V and current window from –100 µA to 10 mA
- Thermal protection
- Internal protection against positive flashover discharges appearing on the CRT.

GENERAL DESCRIPTION

The TDA6107JF includes three video output amplifiers and is intended to drive the three cathodes of a colour CRT directly. The device is contained in a plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package, and uses high-voltage DMOS technology.

To obtain maximum performance, the amplifier should be used with black-current control.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6107JF	DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1

BLOCK DIAGRAM

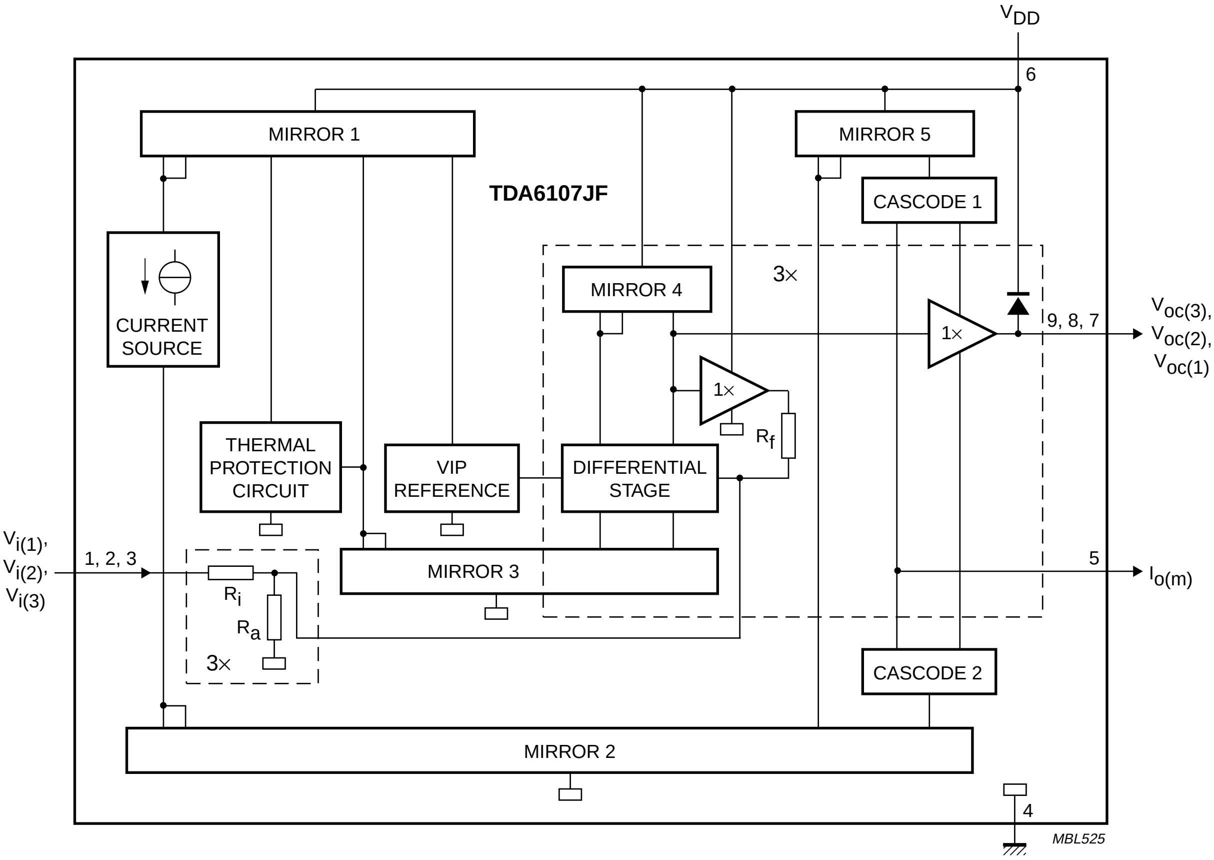


Fig.1 Block diagram (one amplifier shown).

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black-current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1

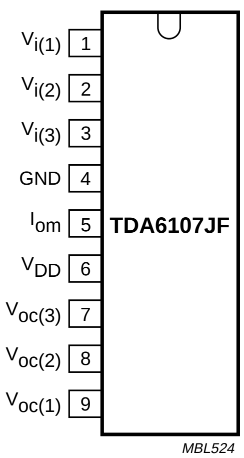


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages measured with respect to pin 4 (ground); currents as specified in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	0	250	V
V_i	input voltage at pins 1 to 3	0	12	V
$V_{o(m)}$	measurement output voltage	0	6	V
V_{oc}	cathode output voltage	0	V_{DD}	V
$I_{ocsm(L)}$	LOW non-repetitive peak cathode output current at a flashover discharge of 100 µC	0	3	A
$I_{ocsm(H)}$	HIGH non-repetitive peak cathode output current at a flashover discharge of 100 nC	0	6	A
T_{stg}	storage temperature	–55	+150	°C
T_j	junction temperature	–20	+150	°C
V_{es}	electrostatic handling voltage			
	Human Body Model (HBM)	–	3000	V
	Machine Model (MM)	–	300	V

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *“Handling MOS Devices”*).

QUALITY SPECIFICATION

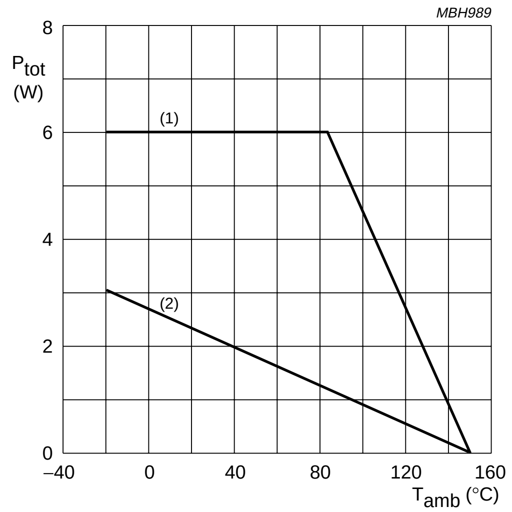
Quality specification *“SNW-FQ-611 part D”* is applicable and can be found in the *“Quality reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient		56	K/W
$R_{th(j-fin)}$	thermal resistance from junction to fin	note 1	11	K/W
$R_{th(h-a)}$	thermal resistance from heatsink to ambient		18	K/W

Note

1. An external heatsink is necessary.



(1) Infinite heatsink.
(2) No heatsink.

Fig.3 Power derating curves.

Thermal protection

The internal thermal protection circuit gives a decrease of the slew rate at high temperatures: 10% decrease at 130 °C and 30% decrease at 145 °C (typical values on the spot of the thermal protection circuit).

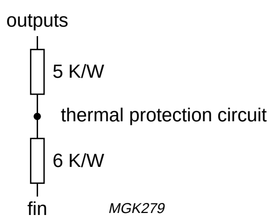


Fig.4 Equivalent thermal resistance network.

CHARACTERISTICS

Operating range: T_j = –20 to +150 °C; V_{DD} = 180 to 210 V. Test conditions: T_{amb} = 25 °C; V_{DD} = 200 V; $V_{o(c1)} = V_{o(c2)} = V_{o(c3)} = \frac{1}{2}V_{DD}$; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); $R_{th(h-a)}$ = 18 K/W (measured in test circuit of Fig.8); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_q	quiescent supply current		5.6	6.6	7.6	mA
$V_{ref(int)}$	internal reference voltage (input stage)		–	2.5	–	V
R_i	input resistance		–	3.6	–	kΩ
G	gain of amplifier		47.5	51.0	55.0	
ΔG	gain difference		–2.5	0	+2.5	
$V_{O(oc)}$	nominal output voltage at pins 7, 8 and 9 (DC value)	I_i = 0 μA	116	129	142	V
$\Delta V_{O(oc)(offset)}$	differential nominal output offset voltage between pins 7 and 8, 8 and 9 and 9 and 7 (DC value)	I_i = 0 μA	–	0	5	V
$\Delta V_{o(c)(T)}$	output voltage temperature drift at pins 7, 8 and 9		–	10	–	mV/K
$\Delta V_{o(c)(T)(offset)}$	differential output offset voltage temperature drift between pins 7 and 8, 8 and 9 and 7 and 9		–	0	–	mV/K
$I_{o(m)(offset)}$	offset current of measurement output (for three channels)	$I_{o(c)}$ = 0 μA; 1.5 V < V_i < 5.5 V; 1.8 V < $V_{o(m)}$ < 6 V	–50	–	+50	μA
$\Delta I_{o(m)}/\Delta I_{o(c)}$	linearity of current transfer (for three channels)	–100 μA < $I_{o(c)}$ < 100 μA; 1.5 V < V_i < 5.5 V; 1.8 V < $V_{o(m)}$ < 6 V	–0.9	–1.0	–1.1	
		–100 μA ≤ $I_{o(c)}$ < 10 mA; 1.5 V < V_i < 5.5 V; 1.8 V < $V_{o(m)}$ < 4 V	–0.9	–1.0	–1.1	
$I_{o(c)(max)}$	maximum peak output current (pins 7, 8 and 9)	50 V < $V_{o(c)}$ < V_{DD} – 50 V	–	20	–	mA
$V_{o(c)(min)}$	minimum output voltage (pins 7, 8 and 9)	V_i = 7.0 V; at $I_{o(c)}$ = 0 mA; note 1	–	–	10	V
$V_{o(c)(max)}$	maximum output voltage (pins 7, 8 and 9)	V_i = 1.0 V; at $I_{o(c)}$ = 0 mA; note 1	V_{DD} – 15	–	–	V
B_S	small signal bandwidth (pins 7, 8 and 9)	$V_{o(c)}$ = 60 V (p-p)	–	5.5	–	MHz
B_L	large signal bandwidth (pins 7, 8 and 9)	$V_{o(c)}$ = 100 V (p-p)	–	4.5	–	MHz
t_{Pco}	cathode output propagation time 50% input to 50% output (pins 7, 8 and 9)	$V_{o(c)}$ = 100 V (p-p) square wave; f <1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 6 and 7	–	60	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Δt_{Pco}	difference in cathode output propagation time 50% input to 50% output (pins 7 and 8, 7 and 9 and 8 and 9)	$V_{o(c)}$ = 100 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3)	–10	0	+10	ns
$t_{o(r)}$	cathode output rise time 10% output to 90% output (pins 7, 8 and 9)	$V_{o(c)}$ = 50 to 150 V square wave; f < 1 MHz; t_f = 40 ns (pins 1, 2 and 3); see Fig.6	67	91	113	ns
$t_{o(f)}$	cathode output fall time 90% output to 10% output (pins 7, 8 and 9)	$V_{o(c)}$ = 150 to 50 V square wave; f < 1 MHz; t_r = 40 ns (pins 1, 2 and 3); see Fig.7	67	91	113	ns
t_{st}	settling time 50% input to 99% < output < 101% (pins 7, 8 and 9)	$V_{o(c)}$ = 100 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 6 and 7	–	–	350	ns
SR	slew rate between 50 V to (V_{DD} – 50 V) (pins 7, 8 and 9)	V_i = 4 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3)	–	900	–	V/µs
O_v	cathode output voltage overshoot (pins 7, 8 and 9)	$V_{o(c)}$ = 100 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 6 and 7	–	2	–	%
PSRR	power supply rejection ratio	f < 50 kHz; note 2	–	55	–	dB
$\alpha_{ct(DC)}$	DC crosstalk between channels		–	–50	–	dB

Notes

1. See also Fig.5 for the typical DC-to-DC transfer of V_I to $V_{O(oc)}$.
2. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

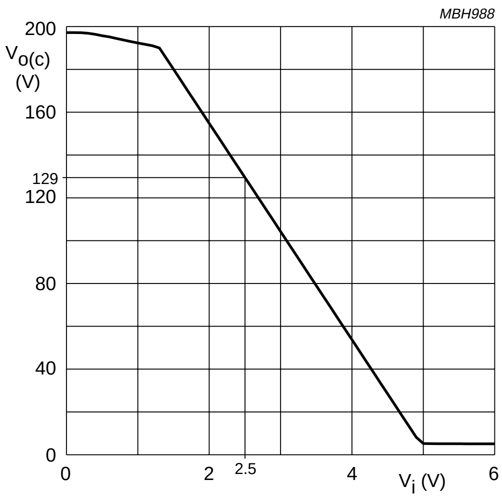


Fig.5 Typical DC-to-DC transfer of V_I to V_{OC}.

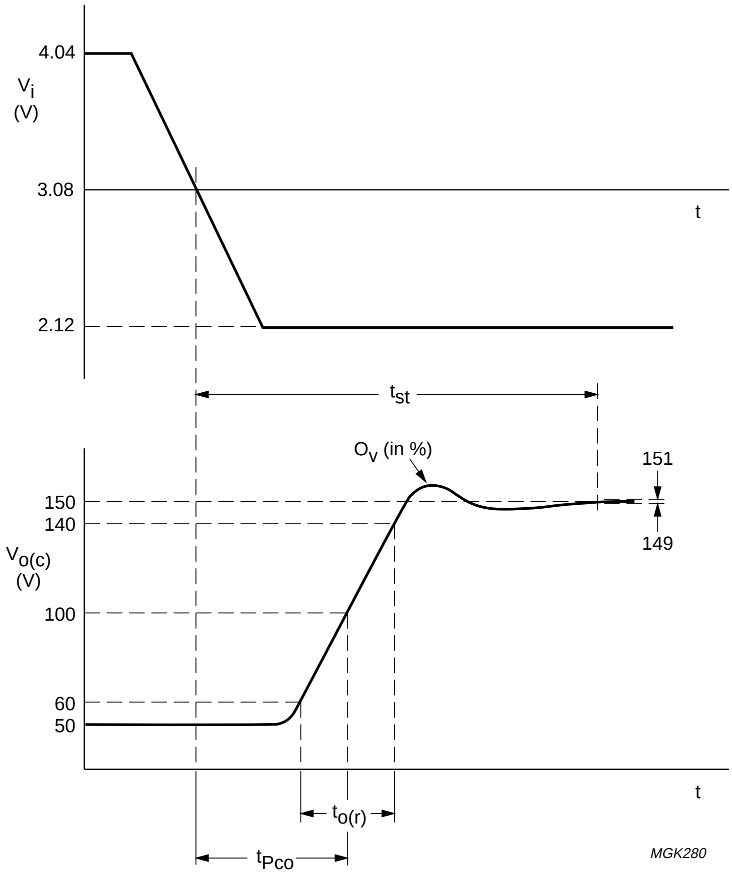


Fig.6 Output voltage (pins 7, 8 and 9) rising edge as a function of the AC input signal.

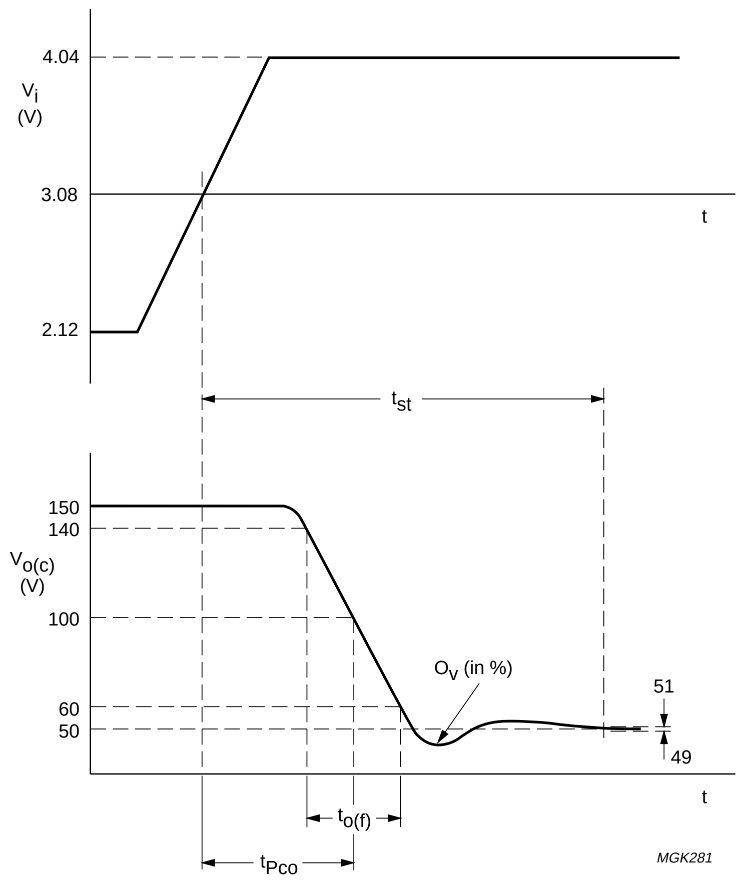


Fig.7 Output voltage (pins 7, 8 and 9) falling edge as a function of the AC input signal.

Cathode output

The cathode output is protected against peak current (caused by positive voltage peaks during high-resistance flash) of 3 A maximum with a charge content of 100 μC [1].

The cathode is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 6 A maximum with a charge content of 100 nC [1].

The DC voltage of V_{DD} (pin 6) must be within the operating range of 180 to 210 V during the peak currents.

Flashover protection

The TDA6107JF incorporates protection diodes against CRT flashover discharges that clamp the cathodes output voltage up to a maximum of $V_{DD} + V_{diode}$.

To limit the diode current an external 1.5 kΩ carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed (for this resistor value, the CRT has to be connected to the main PCB [1].

V_{DD} must be decoupled to GND:

1. With a capacitor >20 nF with good HF behaviour (e.g. foil); this capacitor must be placed as close as possible to pins 6 and 4, but definitely within 5 mm.
2. With a capacitor >3.3 μF on the picture tube base print, depending on the CRT size.

Switch-off behaviour

The switch-off behaviour of the TDA6107JF is controllable. This is because the output pins of the TDA6107JF are still under control of the input pins for low power supply voltages (approximately 30 V and higher).

Bandwidth

The addition of the flash resistor produces a decreased bandwidth and increases the rise and fall times; see *"Application Note AN96072"*.

(1)External protection against higher currents is described in *"Application Note AN96072"*.

Dissipation

Regarding dissipation, distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6107JF is due to voltage supply currents and load currents in the feedback network and CRT.

The static dissipation P_{stat} equals:

$$P_{stat} = V_{DD} \times I_{DD} + 3 \times V_{OC} \times I_{OC}$$

Where:

V_{DD} = supply voltage

I_{DD} = supply current

V_{OC} = DC value of cathode voltage

I_{OC} = DC value of cathode current.

The dynamic dissipation P_{dyn} equals:

$$P_{dyn} = 3 \times V_{DD} \times (C_L + C_{int}) \times f_i \times V_{oc(p-p)} \times \delta$$

Where:

C_L = load capacitance

C_{int} = internal load capacitance (≈4 pF)

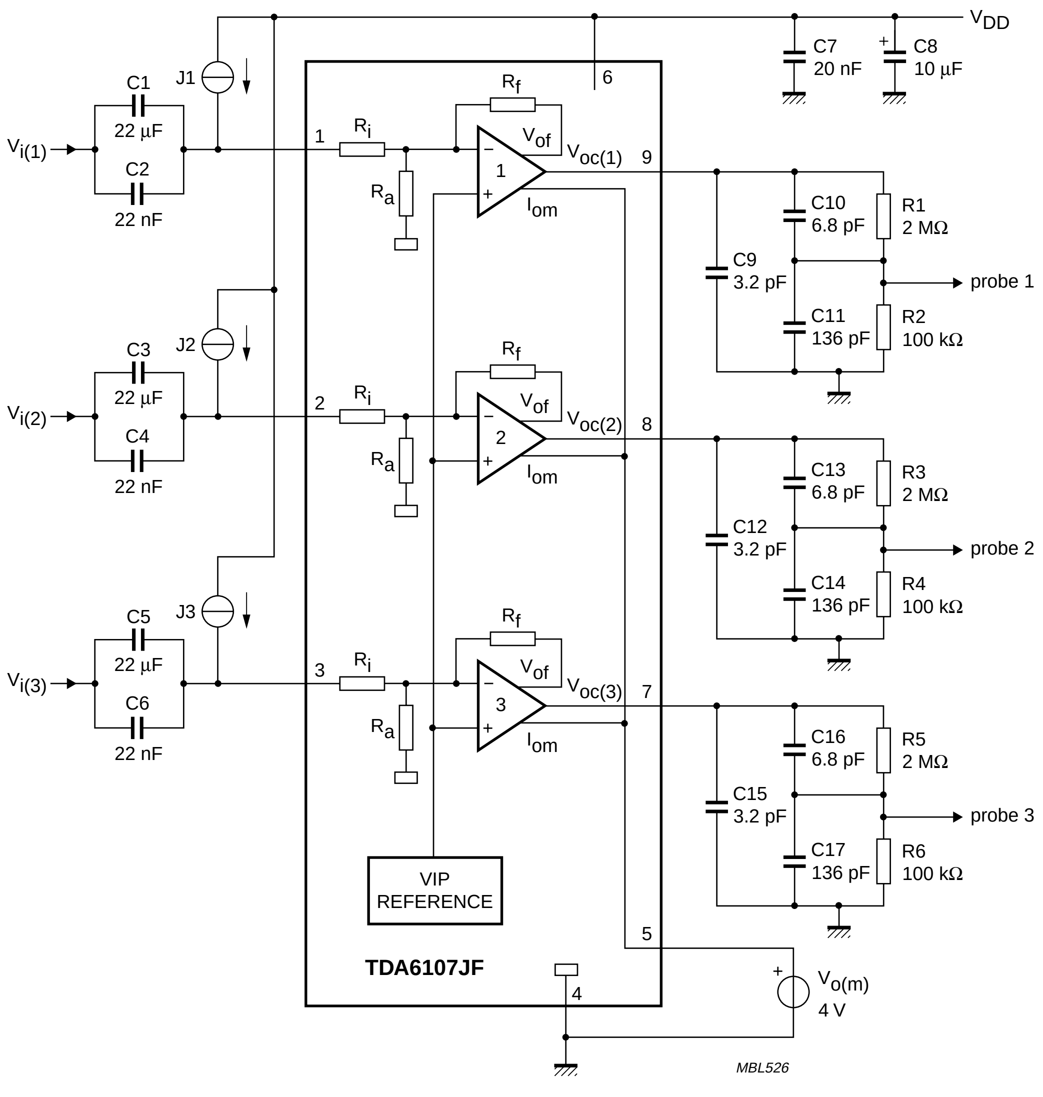
f_i = input frequency

$V_{oc(p-p)}$ = output voltage (peak-to-peak value)

δ = non-blanking duty cycle.

The IC must be mounted on the picture tube base print to minimize the load capacitance C_L.

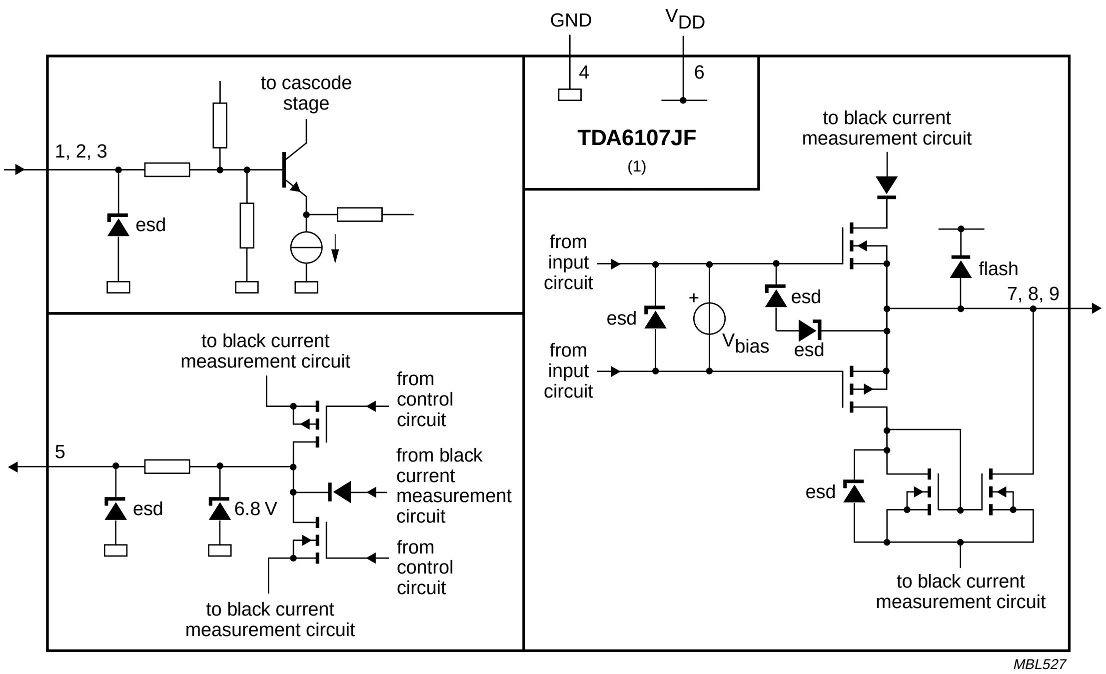
TEST AND APPLICATION INFORMATION



Current sources J1, J2 and J3 are to be tuned so that $V_{o(c)}$ of pins 9, 8 and 7 is set to 100 V.

Fig.8 Test circuit.

INTERNAL CIRCUITRY

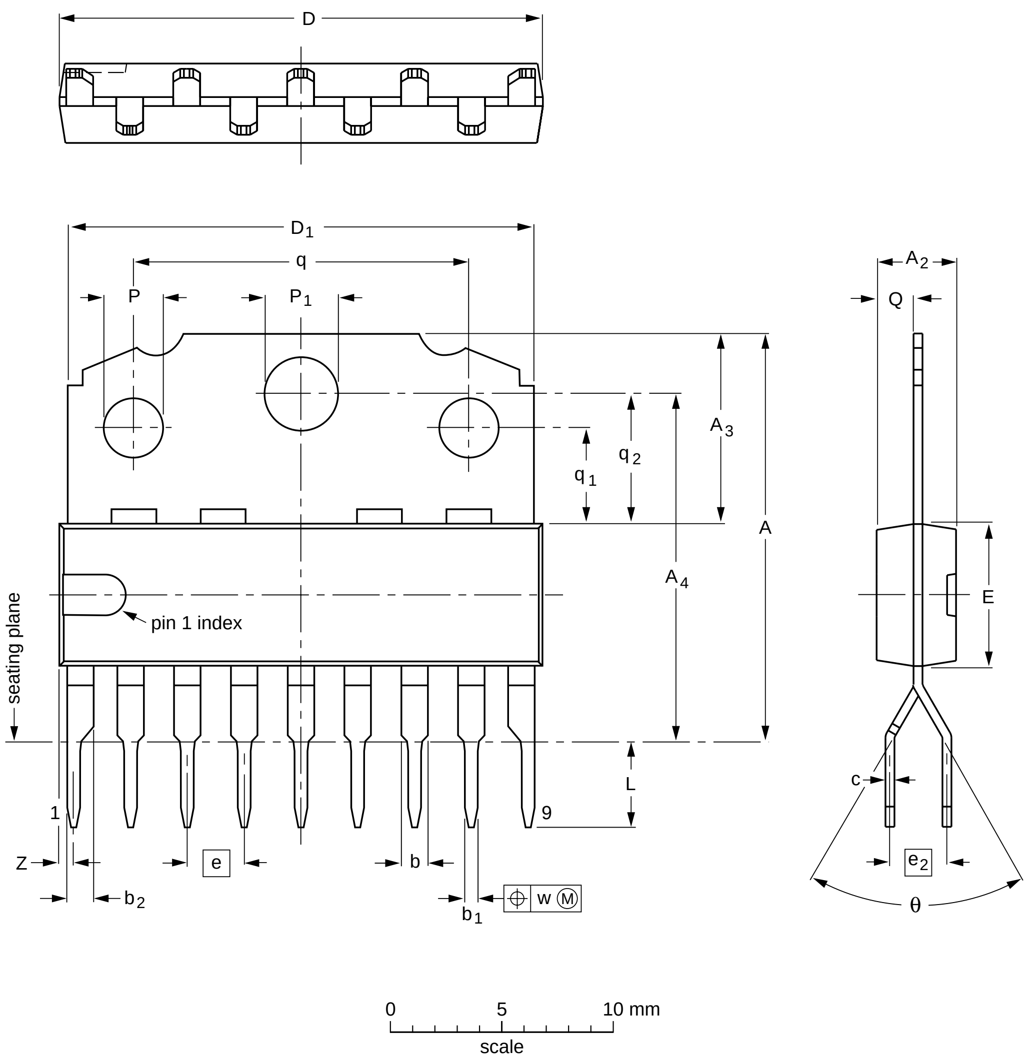


(1) All pins have an energy protection for positive or negative overstress situations.

Fig.9 Internal pin configuration.

PACKAGE OUTLINE

DBS9MPF: plastic DIL-bent-SIL medium power package with fin; 9 leads **SOT111-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	D(1)	D_1	E(1)	e	e_2	L	P	P_1	Q	q	q_1	q_2	w	Z(1) max.	θ
mm	18.5 17.8	3.7	8.7 8.0	15.5 15.1	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0	65^o 55^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT111-1						~~92-11-17~~ 95-03-11

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable(1)

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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